European Patent Office
Europaeisches Patentamt
Office euorpèen des brevets

(11) Publication number: **0 150 325**
B1

(12) **EUROPEAN PATENT**

(10) Patent's date of publication: **September 20, 1989**

(51) Int. Cl.[4]: **H 03 K 5/135**

(21) Application number: **84114396.9**
(22) Application date: **November 18, 1984**

(54) **Delay unit for the production of a delayed output signal**

(30) Priority: **February 2, 1984 DE 3403637**

(37) Assignee: **Siemens, Inc.**
Wittelsbacherplatz 2
D-8000 Munich 2 (GER)

(43) Publication date of application:
August 7, 1985 Patent sheet 85/32

(45) Publication of reference to the patent distribution: **September 20, 1989**
Patent sheet 89/38

(72) Inventor: **Dallmann, Achim,**
Certified Engineer of Physics
Putzbrunner Strasse 18
D-8000 Munich (GER)

(84) Known contract states:
DE FR GB IT NL

(56) Prior art:
EP-A- 0 086 305
FR-A- 2 092 967
GB-A- 2 036 496

Jouve, 18, rue St-Denis, 75001 Paris, France

Description

The inventions suggests a delay unit for the production of an output signal delayed with a definite delay time opposite an input signal, according to a publication by A. Dallmann, "Construction and test of a microprocessor-controlled sampling system for the sub nano-second period," University of Duesseldorf in the year 1982.

Only sampling procedures can be sued for the for the measurement of a fast, electric signal, which means for the regulation of a tension procedure as a function of time, as they are developed, for example, by sampling oscillographs. This measuring principle, namely a tension procedure as a function of time with the aid of a sampling procedure, has also been used, for example, for the measurement of internal signals at integrated cross circuits. This occurs, in this example, with help of an electron ray measuring technique in a grid-electron microscope that has equipment for measuring potential stroboscopic contrast. Such an electron ray measuring device is described, in this case, in the U.S. patent 4,413,181. For the stroboscopic operation in such an electron ray measuring device, a delay unit has been necessary for fixing the measurement time at a very high accuracy. With an electron ray measuring device, such a delay unit should also be calculatable over and above that, and a high repetition rate should be made possible with the keying in of the electron rays. Delay units with very high time-precision that permit a high repetition with the measurement of fast signals, have been necessary in each sampling system.

For the representation of the tension procedure as a function of time in cyclically working, integrated circuits, stroboscopic diagrams have been used for the electron ray measuring technique. Therefore, a pulsated electron probe, synchronous with the cycle of the tension procedure, has been adjusted to a circuit node inside of an integrated circuit on one or more of such circuit nodes. For very high frequency tension procedures on such circuit nodes, a high repetition rate of the electron probe is necessary.

Earlier, a boxcar integrator, i.e. Model 162 of the company, Princeton Applied Research, has been used for electron ray measuring devices (see the aforementioned U.S. patent no. 4,413,181), which the phase advancement has

been achieved for the pulsated electron probe and for the measuring signal process, with regards to the tension procedure for a circuit node of a measuring object above an analogous ramp generator with an unswitchable increase time and, thus, with a constant, relative accuracy of 0.05%. This means an accuracy of the delay time and/or a time resolution of app. 5 ns, with delay times of 10 µs between the input signal of the delay unit, in this case the start cycle of a cyclic tension procedure, and the output signal for the production of an electron pulse and/or a gate signal for the processing of a measuring signal.

When changing a measuring area while using such a boxcar integrator, this device must be switched off by hand. With the use of a boxcar integrator, computer control is, therefore, possibly only definite within its own measuring area. The maximum repetition rate of such a boxcar integrator amounts to 2 MHz, whereby the repetition rate is marked by the processing speed in the device, especially by the trigger process and ramp control.

Meanwhile, accuracy of a delay unit and/or time resolution of app. 5 ns and a maximum repetition rate of 2 MHz are no longer attainable for many application cases with the electron ray measuring technique.

From the dissertation, "Construction and test of a microprocessor-controlled sampling system for the sub nano-second period" by A. Dallmann, University of Duesseldorf, Germany, October 1982, a method and delay unit are known prior art for the production of a delayed output signal. In a delay unit, according to this dissertation, the delay unit has been implemented in rough steps of 20 ns by a count of a 50 MHz quartz signal. A narrower division of the delay time has been achieved by a fast ramp signal with a border resolution of less than 0.5 ns. With a delay unit, according to this dissertation, the signals of such a quartz generator, which should exhibit and attainably frequency stability, are not synchronizable with the input signal. Therefore, with a delay unit according to this dissertation, the input signal starts, first of all, the sequence of a fast ramp signal. Thus, this sequence of the fast ramp signal has, however, been interrupted during a pre-selected count time of a 50 MHz counter. At the end of this pre-selected count time, the fast ramp signal finally attains a planned reference tension and therefore releases the delayed output signal of the delay unit. The

reference tension used for the ramp signal can be implemented by a computer with a digital-analog converter. The pre-selected count time and the reference tension used for the ramp signal can also, however, be provided without the use of a computer with the help of another device.

With a delay unit according to the named dissertation, both the application of a new counter condition and also the loading of each new counter condition such as the start of an operation mode of the delay unit, in which the next incoming input signal releases the next delayed output signal, have been controlled by the computer. The controlling of this operation procedure of the delay unit between two delayed output signals is extensive and lengthy. This controlling of the operation procedure by the computer limits the maximum repetition rate of the delay unit.

In GB-A- 2 036 496, "Pulse delay circuit," a delay circuit that includes a count step is likewise provided. Through a start impulse to the input of the delay circuit, a RC circuit has been made herewith and by a flip-flop stem of the counter. As it can be inferred from the description concerned, the uploading of a capacity in the RC unit has been interrupted by the count process in the count step, whereby after the completion of the count process, the uploading process has been determined. Finally, the desired delayed signal has been released at the end of the uploading process by a pulse generator for the output of the delay circuit. According to the specification in the patent application concerned, this delay circuit permits a minimum delay time of 100 ms. This is, however, likewise not attainable for many application cases in the electron ray measuring technique.

The present invention outlines the task of providing a delay unit of the prior art for the production of a delayed output signal, which possibly permits reasonably higher repetition rates as those according to the current state of technology.

This task has been solved, according to the invention, by a delay unit according to claim 1. Implementations and advantages of the invention are represented in the description and the figures.

With a delay unit according to the invention, a new, pre-selected count condition has been refreshed automatically, which means independent of a computer, after each delayed output signal in a counting component. In this

way, repetition rates of, in this example, 20 MHz have been made possible. A delay unit, according to the invention, therefore satisfies, in this example, the requirements that have been used in the electron ray measuring technique for such a method and for such a delay unit. The delay unit, according to the invention, can also be inserted into other measuring systems besides the electron ray measuring technique for the analysis of fast signals where an overall high repetition rate is necessary or advantageous.

A delay unit, according to the invention, makes a constant, absolute time accuracy of 0.5 ns possible, both with short and also with long delay times. Beyond that, the delay unit, according to the invention, makes possible a minimum delay unit of app. 15 ns between signal input and signal output. It is advantageous with many measuring systems, if they can be controlled by a computer. The delay unit, according to the invention, makes a simply controlling by a computer possible.

Implementation examples of the invention are represented in the following figures and have been more clearly explained in the following.

Fig. 1 shows a block circuit diagram of a delay unit, according to the invention.

Fig. 2 shows a signal diagram for a method and for a delay unit, according to the invention.

Fig. 3 shows an implementation example for a delay unit, according to the invention.

Fig. 1 shows a delay unit according to the invention. The input signal (trigger) 1 meets with an input of a comparator 2, in the second input of which lies a trigger threshold 3. As soon as the output of this comparator 2 has been implemented by a particular tension level, this output of the comparator 2 has been locked so that this output signal of the comparator 2 also remains preserved after the fading out of the same input signal, which has caused the implementation of this output signal from the comparator 2 at a particular tension level. The output signal of the comparator 2 is thus connected with a 50 MHz prefix counter, such that this prefix counter 4 can be arranged by the output signal of the comparator 2 to count by an implemented counter condition after zero. The pre-selected counter condition for this prefix counter 4 has been provided by a computer with an MPU bus 11 and further worth a signal direction 13 between the bus 11 and the prefix counter 4. A 50 MHz generator provides the

time, to which the 50 MHz prefix counter 4 counts by the pre-selected counting condition.

The output signal of the comparator 2 and the output signal of the prefix counter 4 have been joined together for the control signal of a ramp generator 6. The output signal 16 of the ramp generator 6 has been compared with reference tension 15 by another comparator 7. The size of the reference tension 15 can be provided by a computer with the MPU bus 11 and with signal directions 12 between this bus and a digital-analog converter and further with this digital-analog converter. With the output of the comparator 7, the delayed output signal 9 appears. This delayed output signal 19 has been returned to the prefix counter by a signal direction.

Fig. 2 shows a signal diagram for a delay unit according to the invention. The input signal 1 shows a positive flank for the time t=0. The output signal 14 of the quartz generator is not, according to the phase, correlated with the appearance of the input signal 1. The positive flank of the input signal starts the sequence of the ramp signal 16 by the control signal 17, which has been formed in this case by the output of the comparator 2. Soon after the appearance of the input signal 1, the first positive flank of the quartz signal appears. The control signal 17 for one has been set with an output of the prefix counter 4 and the sequence of the ramp signal has been interrupted so that the ramp signal 16, subsequently, retains the same value that it had exhibited with the appearance of the first positive flank of the quartz signal 14 after the implementation of the input signal 1.

With the appearance of the first positive flank of the quartz signal 14 after the arrival of the input signal 1, the programmable prefix counter 4 that counts from the counter condition implemented after zero has been allowed. The time for this counting of the counter condition implemented after zero has been formed by the quartz signal 14. The counting time of the prefix counter 4, therefore, amounts to t_z. The quartz signal 14 has been produced by a 50 MHz generator 5. Thus, the timely interval between two pulses of this quartz signal amounts to 14 20 ns. The pre-selected counter condition in the prefix counter 4 includes n beats of the quartz signal 14. Thus, the counting time amounts to t_z n.20 ns. After the sequence of the counting time t_z of the prefix counter 4, the interruption of the ramp signal 16 has been cancelled. After a time

T, a ramp signal 16 thus continues to change itself with a broader time span $T + t_4$ so that it attains the time $T + t_4$ for the value of the reference tension 15. As soon as the ramp signal 16 attains this value of the reference tension 15, the delayed output signal has been released. This delayed output signal has been directed back to the prefix counter 4at the same time as the signal 10, where this signal 10 causes the loading of a new counter condition into the prefix counter independent from the computer.

The value of the reference tension 15 lies between the tension U and a tension U_{T+20}. This tension U_{T+20} would have been achieved by the ramp signal 16 after the course of a time & + 20 ns. The ramp signal 16 achieves the value U independent of the phase situation of the quartz signal 14, as a result of the phase situation of the input signal 1 and independent of the counter condition of the prefix counter 4 for the time T. In the time interval between the time T and the time T + 20 ns, the refined division of the complete delay time occurs. Therefore, the reference tension 15 must lie between the tension U for the time T and the tension U for the time T + 20 ns.

For delay times smaller than 40 ns, the counting method cannot be used. Fro delay times smaller than 40 ns, the counter has been switched off and a purely analogous delay has been implemented. Therefore, the sequence of the ramp signal 16 has been started by the positive flank of the input signal 1 with the output signal of the comparator 2. This ramp signal 16 proceeds, then, without interruption, until the value of the ramp signal 16 attains the value of the reference tension 15 and, therefore, releases the delayed output signal 9.

Fig. 3 shows an implementation example for the delay unit according to the invention. In a circuit for a delay unit, according to the invention, short increase times and delay times and/or jitter must most possibly be able to be attained, thus observing the following: With a high ohmic construction, longer uploading times can already appear through nearly unavoidable direction capacities of their own pF. In this example, the time constant, which can be set as the product of resistance and capacity, amounts to 20 ns with a resistance of 1 kOhm and a capacity of 20 pF. Further, the construction of the circuit for the delay unit, according to the invention, must most possibly take place with low induction. Components with high inductive

parts like wire resistors or electrolyte condensers, for example, may not be used in critical component groups. Beyond that, the semiconductors used must exhibit low suspendable layer capacities and high marking frequencies and, therefore, short increase times. The demands, which are positioned on diodes and transistors for these reasons, have, however, already been fulfilled by simple construction types like, for example, 1 N 914, BC 237, BC 307, etc. With such simple construction types, circuit times can already be achieved in 2-3 ns.

Furthermore, observing the following with the circuit conception: Only a short delay occurs with the switch of pn-transition to the condition suspended in the direction. Therefore, the freeload carrier of the suspending layer must be emptied from one and the suspending layer capacity must be uploaded with the load resistance from another. Therefore, the load resistance may not be too great such that the provided suspending layer capacity of approximately 10 pF can be uploaded fast enough. Additionally, the count of the freeload carrier must most possibly be held low in the suspending layer, at least so it must be seen to that no operation of the suspending layer occurs in the saturation layer.

Because with a suspending layer in the saturation area, an overflow of the suspending layer instead occurs with freeloading carriers. The conductivity of the superconductive switch element is indeed very good, but when switching to the suspended condition, a freely occurring time additionally appears that can amount to about 10 µs with small direction transistors.

For the integrated components that have been used in a delay unit according to the invention, the same demands are being posed as for the discrete components. With the construction of the circuit, DCL-IC's (series 10000) and ECL comparators (high speed comparator SP 9685) have been used in the critical component groups because the other series of integrated components are not fast enough.

The construction of the circuit should be inductively low without great interferences and reflections. In order to achieve this, sides of platinum can be considerably formed as mass sides an be laid near the signal paths as mass paths. Therefore, small induction and a definite imposition with the appropriate width of the direction paths (micro-strips) can be attained. Details with regard to ECL components may be

inferred from the book, "MECL High Speed Integrated Circuits," Motorola Semiconductors (1978).

The control of a delay unit, according to the invention, takes over a micro-processing system. In the implementation example, a multi-carded system with commercially accepted cards (MPC) has been chosen. To it belongs a MPU card MPC 103 with a microprocessor 6802 (Motorola) with a 16 kbyte EPROM and with a 2 byte RAM. Two-piece, 8 byte RAM cards MPC 112 also belong to it. A teleprinter Teletype model can serve as an input medium that can be closed by a serial interface MPADA 04A (TTY interface). Therefore, an input is possible with the keyboard of the teleprinting machine and an output is possible with the printer. A 9-inch monitor can serve as another output medium that can be accessed by a card MPC 402 (video interface). A magnetic band device type DCD 1 (3M Company) can serve as another output medium that can be accessed by another interface card MPC 250. A Plotter Watanabe Digiplot can serve as another output medium that can be accessed by another interface card MPC 250.

This micro-processing system controls a delay signal, according to the invention, by a MPU bus 11 with the help of the control signals 12, 13. The control signals 12 proceed to the digital-analog converter 8 for the reference tension. The digital-analog converter 8 is created from a card MPC 124. The control signals 13 proceed to the prefix counter 4, which is essentially created from the ECL counter Z1 and the TTL counter Z2 in the implementation example according to Fig. 3.

In a very simple implementation form, a delay unit, according to the invention, must not necessarily be controlled by a micro-processing system. Any device, which can output the signals 12, 13 in definite ways to a delay unit according to the invention, is basically enough to control a delay unit according to the invention.

In order to achieve a constant accuracy with the exact time scale for the delay time under 1 ns possible and in order to make a calculated control of the delay time possible, the following principle has been chosen: The delay time period has been roughly divided up into steps by the counting of a signal 14. A refined division of the delay time period between each two steps of the rough division takes place with the help of a ramp generator 6, of which momentary

amplitude 16 has been compared with a provided comparison tension.

The 8-bit digital-analog converter 8 makes possible a minimum release of 0.1 ns with the refined division of a time period of 20 ns. This lies clearly with the release of the other components into the circuit according to Fig. 3. With an accuracy of the signal 14 of app. 10^{-5}% and with a linearity of the ramp generate 6 at better than 1%, an accuracy of better than 0.5 ns with the define delay time period is, therefore, expected. The ramp generator 6 has been, thus, continually run with the same input time; switch elements have, therefore, not been necessary.

For the production of the signal 14, a 50 MHz quartz generator 5 has been used. The signal 14 has been produced by an oscillator circuit in Fig. 3 that resonates with approximate tuning of a resonant circle at 50 MHz, reliable on the overflow. Details of this circuit are found in the application report for TTL integrated circuit boards by Texas Instruments. The circuit for the production of a signal 14 exhibits an uncoupling stage with this. This uncoupling stage prevents the loading of the resonant circuit and strengthens the signal amplitude of the signal 14 at a tension of app. 3 V_{SS}.

In the digital part of the circuit according to Fig. 3, the following components have been used: SP 9685 high speed comparators 2, 7 each with a latch (lock). The outputs of these comparators 2, 7 exhibit ECL levels. The comparator 2 has been necessary for the preparation of an input signal 1 and the comparator 7 has been necessary for the comparison of the ramp signal 16 with the reference tension 15.

An ECL counter MC 10136 serves as the counter Z1. This counter Z1 has been used in the first counting stage as a programmable, synchronized 4-bit prefix counter up to 100 MHz.

A TTL counter 74LS191 serves as counter Z2. This counter Z2 has been used in the second counting stage as a programmable, synchronized 4-bit prefix counter up to 5 MHz.

An ECL dual D flip-lop MC 10231 serves flip-flop FF1. This flip-flop FF1 has been used for the control of the ramp generator 6.

ECL OR Gates 10103 4 x 2 OR gate has been used for gates N1, N2, N3, N4, N7. ECL OR Gates MC 10109 4/5 OR/NOR gates have been used for gates N5, N6.

With a positive tension jump of the input signal 1, the output Q of the comparator 2 has been set at the logic value 1. The comparator 2 has been locked by gate N1 so that the output signal of the comparator 2 remains preserved after the fading out of the positive tension jump of the input signal 1. Thus, a logic "1" fits closely with the D-input of the flip-flop FF!. With the next positive flank of the signal 14, the output Q of the flip-flop FF1 has also been set at the logic value "1." At the same time, the counter Z1 maintains a carry-in signal of this flip-flop FF1 and begins to count by the second positive flank of the signal 14 from the implemented counter condition. The counter Z1 has, thus, first been allowed, if the flip-flop FF1 is already switched. In the implementation example according to Fig. 3, the counter Z1, thus, first counts the second impulse of the signal 14 after the appearance of the positive flank of the input signal 1. This circuit principle prevents an erred correlation between input signal 1 and signal 14 where, under known conditions, one of both integrated circuits FF1 already switches Z1 while the other of both these integrated circuits FF1 has, however, first switched Z1 at the next beat impulse. Because the counter Z1 in a circuit according to Fig. 3 – thus in contrast to the signal diagram according to Fig. 2 – first counts the second impulse of the signal 14, the counter condition, which has been set in the prefix counter 4 by the signals 13 in a circuit according to Fig. 3 around 1, must be lower in comparison to a circuit, with which the signal diagram according to Fig. 2 is realized.

The counter Z1 counts the four lower-value bits of the counter condition provided by the signals 13. The counter Z2 counts the four higher-value bits of the counter condition provided by the signals 13 with the converters K1, K11. Converters ECL-TTL MC 10125 and/or TTL-ECL MC 10124 can be used for converters.

At the counter condition "0," the outputs Q0-Q3 of the counter Z1 are each set at the logic value "0," which exhibits the min-max output of the counter Z2, in this case the logic value "1." Thus, the inverted output of the gate N5 has also been set, in this case, at the logic value "1," because all inputs of the gate N5 in this case each exhibit the logic value "0," and consequently, the flip-flop FF1 has also been reset. The output signal Q of the flip-flop FF1 and the inverted output signal of the comparator

2 have been joined together at the gate N2 by the control signal 17 of the ramp generator 6. At the same time as the reset of the flip-flop FF1, another flip-flop FF2 has been set and by it, the time signal of the flip-flop FF1 has therefore been blocked. Through this, it has been presented that the signal 14 can cause a further switching of the flip-flop FF1.

For delay times under 40 ns, a logic "1" has been set at the input X1 of the converter K12 by the signals 13 and, likewise, the counter condition has been set at "00." Thus, the flip-flop FF1 and the flip-flop FF2 have been blocked by the gate N3 and the counters Z1, Z2 have been made passive. The input signal 1 ahs been directed directly to the ramp generator 6 by the gate N2, in this case for delay times under 40 ns, and thus without timely interruptions.

The setting of each new counter condition for the inputs of the counter Z1, Z2 happens in the micro-process from between the arrival of an input signal 1 at the input of the delay time, provided that this input signal 1 switches the output Q of the comparator 2 to the logic value "1" an thus cases a locking of the output signal of the comparator 2, and at the arrival of another input signal 1, which can switch after passage of a delayed output signal 9 at the delay unit for the next input signal 1, again with the output Q of the comparator 2 at the logic value 1. This setting of a new counting condition for the inputs of the counters Z1, Z2 has been caused by the inverted output of the comparator 2 by an inverted converter K3 with a trigger signal X5. The trigger signal X5, therefore, releases into the micro-processing system the sequence of the setting of the new counting conditions for the data inputs d0, d7 of the counters Z1, Z2. The inputs T1, T2 each continually exhibit the logic value "0."

The signal 10, which corresponds to the inverted delayed output signal, forms both the inputs of the gate 7 as well as the signal T1. As long as the signal 10 exhibits the logic value "1," thus as long as the delayed output signal 9 for the output of the comparator 7 has still not appeared, the counting conditions newly set for the inputs d0, d7 of the counters Z1, Z2 has not been accepted into these counters. As soon as the signal 10 accepts the logic value "0," which means as soon as the delayed output signal 9 appears for the output of the comparator 7, both inputs of the comparator 7 exhibit the logic value "0." This setting of both the inputs S1, S2 for the counter Z1 has five consequences:

1. the four lower-value bits d0, d3 of the new counter position have been accepted into the counter Z1,
2. the counter Z2 has been controlled by the gate N6 and by the converter K2, and the four higher-value bits d4, d7 of the new counting condition have been fed into the counter Z2,
3. the flip-flop FF2 has been reset by the inverted output of the gate N6,
4. likewise the latch-circle of the comparators 2,7 with the gates N1, N4 have been reset by the inverted output of the gate N6,
5. the load condenser C1 has been unloaded by transistor T4 in the ramp generator 6.

Immediately after the fading out of the delayed output signal 9, the signal 10 again exhibits the logic value "1." This means that the input S1 of the counter Z1 once more exhibits the logic value "1," while the input S2 of the counter Z1 continues to exhibit the value "0." Therefore, the operation mode "countdown" is set for the counter Z1. Then, the next delayed output signal 9 has been released by the next positive tension jump of the input signal 1.

The invention makes possible an automatic, computer-independent loading of a new counting condition in the prefix counter 4 and an automatic, computer-independent preparation condition of the delay unit of which a newly appearing input signal 1 releases another delayed output signal 9. Thus, high repetition rates of the specific measuring system have been made possible. In the electron ray measuring technique, it is necessary, in this example, that a cycle of a periodic tension procedure has been fully recorded in a measuring object in the most possibly short time. Such a recording of a cycle of a periodic tension procedure occurs with the help of the sampling principle. In order to be able to extract a timed-release from the cycle of a periodic signal procedure, the phase, with which the electron probe has arisen as a result of the cycle of the periodic signal path leaving from a circuit node, has thus been varied by the different measuring impulses.

The electron probe has thus been periodically pulsed at the circuit node for the period of the recording tension procedure. Each pulse of the electron probe exhibits, therefore, another phase as a result of the cycle of the recording tension procedure. If the phase of the pulsed electron probe as a result of the periodic signal path being

recorded had been shifted by the specific cycle of this signal path being recorded, an entire cycle of the periodic signal path being considered has been recorded by the measuring signal process. The sampling principle in the electron ray measuring technique has been described, in this example, in the U.S. patent 4,220,853.

The measuring signal process can take place with a measuring according to the sampling principle with the help of a time window (gate). The time release of a measurement has then been clarified by the gate time of the time window and by the accuracy of the time, to which the pulsed electron robe arises with each of a defined delay time (phase) at a circuit node. Therefore, it does not, thus, verily arise at the absolute accuracy of the delay unit as much as at the reproduction (jitter) of this delay time. Synchronous with the pulsed electron probe, the gate of the measuring signal process has also been controlled by the delayed output signal 9.

If, in this example, the delay times (phases) of the pulsed electron probe in the electron ray measuring technique as a result of a periodic tension procedure always being considered in the same defined ways, has been varied, the signals 12, 13 have also been released by a relatively simple switching of the counter. In such a case, a costly micro-processing system has not been absolutely necessary.

With a delay unit according to the invention, the input signal 1 goes through two singular components to the ramp generator 6, namely the comparator 2 and the gate N2. Therefore, a very short delay time of app. 4 ns has been achieved up until the start of the ramp generator 6.

The ramp generator is created from the following components:

- a constant flow source at the integrated circuit IC1 and the transistor T5,
- a switch at the transistor T3,
- a loading stage at the transistor T4,
- an uncoupling stage at the transistor T3,
- a preparation of the reference tension at the integrated circuit circle IC2 and with a comparison step at the comparator 7 and the gate N4.

Independent of the tensions on the base electrodes of the transistors T1, T2, the constant flow by the collector of the transistor T5 flows out either into the load condenser C1 or at the resistance R3. The tension of the base of the transistor continually amounts to app. -7.5 Volts. With the resistances R5, R6, R7, the control signal 17 for the ramp generator 6 has been brought to the correct level: The logic "1" corresponds with a tension of -7.1 Volts and the logic "0" corresponds with a tension at -7.9 Volts. With a logic "0" for the output of the gate N2, the load condenser C1 has thus been loaded. At a logic "1" of the control signal 17, the load condenser C1 holds the momentary tension value. The ramp signal 16 arrives at the source follower T3 for the inverted input of the comparator 7. The ramp signal 16 can there accept a value between +2.5 Volts and -5.7 Volts. Therefore, the tension U, which accepts the ram signal for the time T, amounts to 0.6 Volts. The DC comparison tension 15 must, therefore, thus accept values between 2.5 Volts and 0.6 Volts for delay times greater than 20 ns in order to simplify the comparison process. This following measurement must be realized: For delay times smaller than 20 ns, the counts of 00-7F for the input of the digital-analog converter 8 have been used and for delay times greater than 20 ns, the counts 80-FF have been used. Therefore, the signal X1 has no longer been necessary for delay times smaller than 40 ns. A constant tension at the zero point position has been added on for the output signal 15 of the digital-analog converter 8. Thus, one can implement the constant flow by the potential gauge P1, the zero-point of the reference tension 15 by the potential gauge P3, and the strengthening of the reference tension 15 by the potential gauge P4.

The comparator 7 compares the ramp tension 16 with the reference tension 15 and delivers an ECL-tension jump as a delayed output signal 9.

A TTL signal as a gate signal can arrive at a converter K10 by a measuring signal process mechanism.

Provided that an achievable, frequency-stable input signal 1 is present, this input signal can be synchronized with the signal 14. Such a synchronization makes it possible for the sequence of the counting process in the prefix counter to be directly released by the input signal 1 and for the first closing of the ram generator 6 to be controlled without timely interruption up until the ramp signal 16 has attained the value of the reference tension 15.

Claim

Delay unit for producing an output signal (9) which is delayed by a defined delay period ($T + t_x$) compared with an input signal (1), consisting of

— a comparator (2), at one input of which the input signal (1) is present and at the second input of which a trigger threshold (3) is present,

— a preselection counter (4) for setting the delay period ($T + t_x$) step by step, an output signal of the comparator (2) being present at an enable input of the preselection counter (4) and a count being predetermined at this preselection counter (4) by a computer via a bus (11) and further via signal lines (13),

— a constant-frequency signal generator (5) for emitting counting pulses (14) to the preselection counter (4),

— a ramp signal generator (6) for finely dividing the delay period ($T + t_x$), an output signal of the comparator (2) and an output signal of the preselection counter (4) being combined to form the control signal of the ramp signal generator (6) and an output signal (16) of the ramp signal generator (6) being generated at the output of the latter, the sequence of the output signal (16) of the ramp signal generator (6) being interrupted with the first positive edge of the counting pulses (14) to the preselection counter (4) after arrival of the input signal (1) and the preselection counter (4) being enabled,

— a device (8) for generating a reference signal (15) for the output signal (16) of the ramp signal generator (6), in which arrangement the magnitude of the reference signal (15) can be predetermined by the computer via the bus (11) and further signal lines (12) to the device (8),

— a further comparator (7) in which the output signal (16) of the ramp signal generator (6) is compared with the reference signal (15) and which emits the delayed output signal (9) at its output,

— and a further device (10) for feeding back the delayed output signal at the output of the further comparator (7) to the preselection counter (4) for automatically loading a new count into the preselection counter (4) independently of the computer.

FIG 1

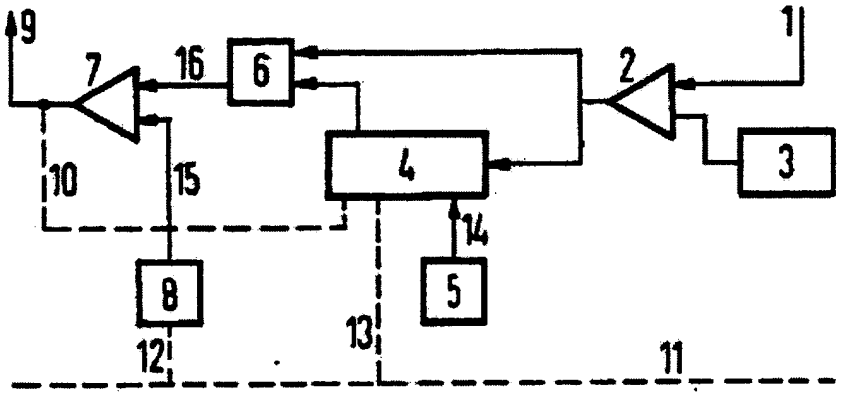
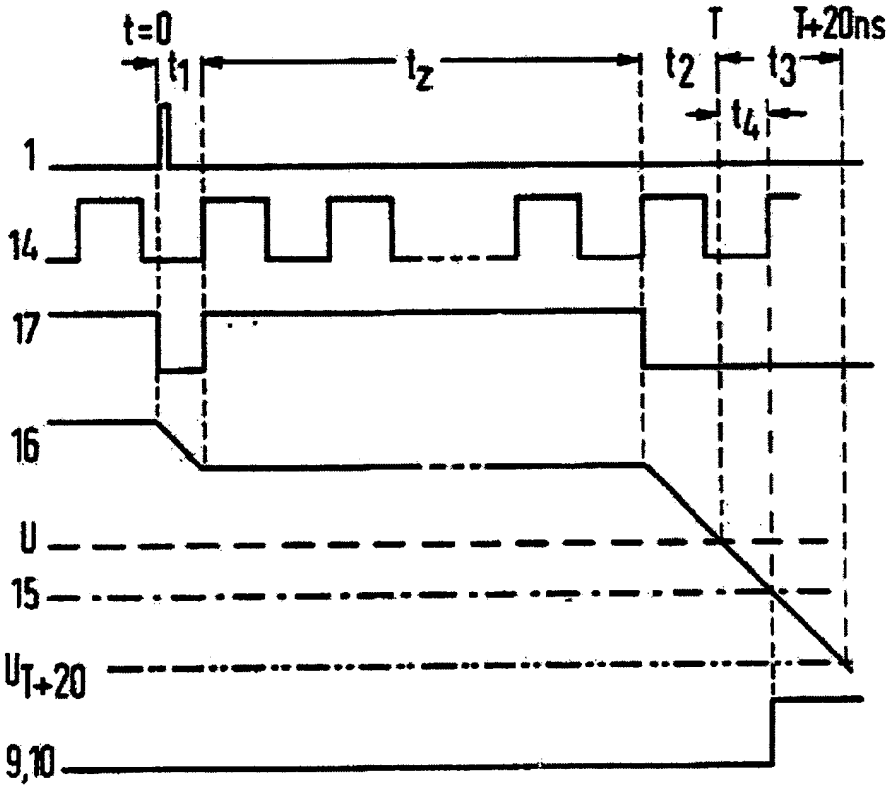


FIG 2



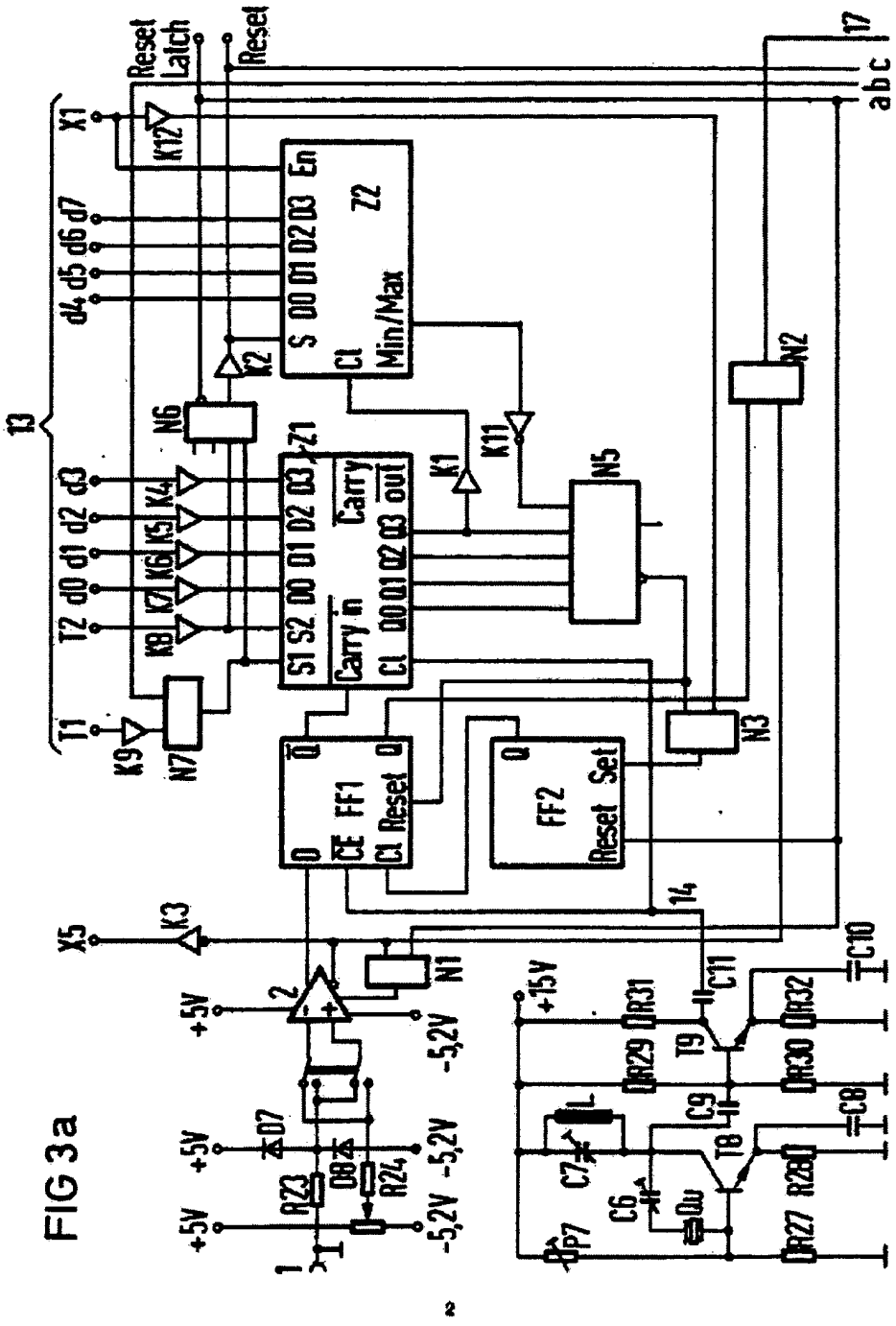

Reset Latch
Reset
X1
K12
d4 d5 d6 d7
S D0 D1 D2 D3 En
Z2
Min/Max
C1
K2
N6
T3
Z1
K4
K5
K6
K7
K8
T2 d0 d1 d2 d3
S1 S2 D0 D1 D2 D3
Carry
Carry in
C1 Q0 Q1 Q2 Q3 out
K1
K11
N5
N2
T1
K9
N7
N3
D
CE FF1
C1 Reset
FF2
Reset Set
14
17
a b c
X5
K3
N1
+5V
-5,2V
+15V
R31
C11
C10
R32
T9
R29
R30
C9
C8
T8
C7
C6
R28
R27
P7
R23
D7
D8
R24
1
2

FIG 3a

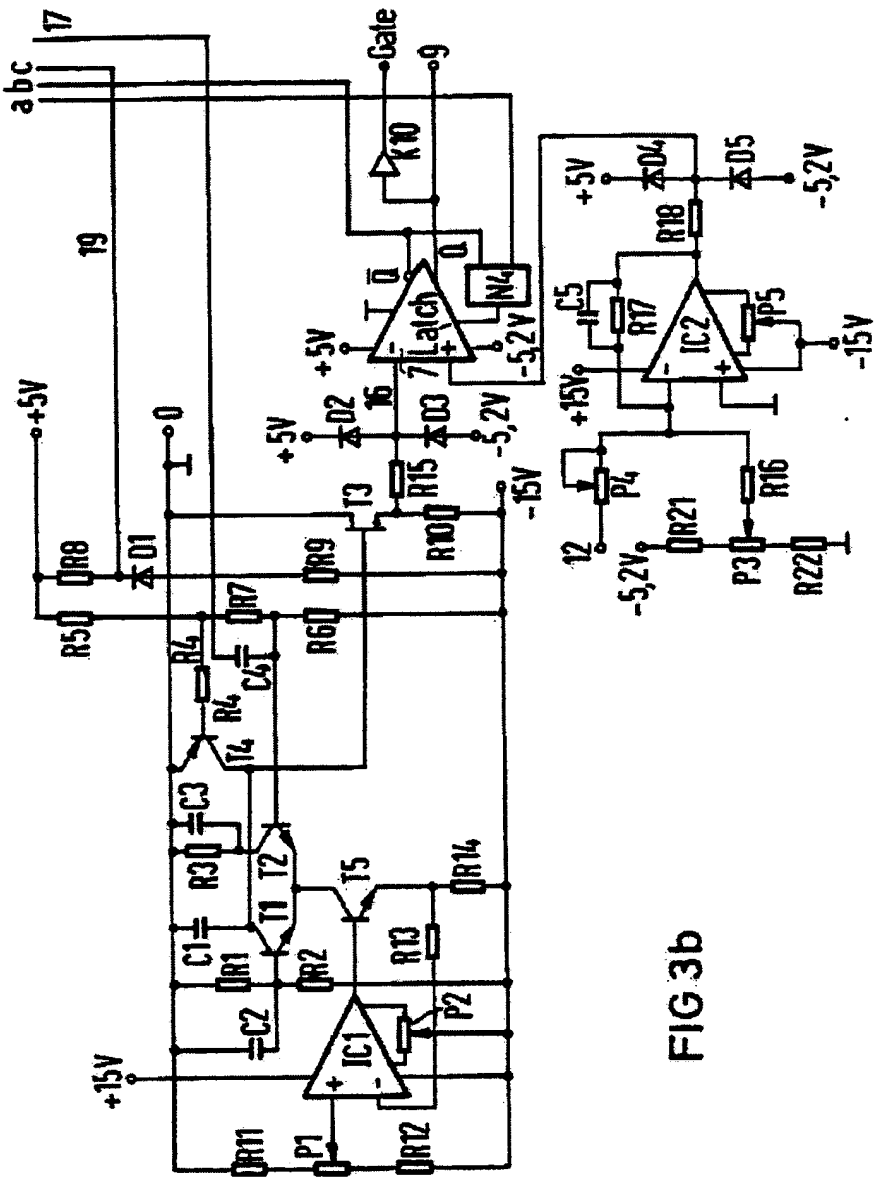

17
a b c
19
Gate
9
K10
Q̄
Q
N4
Latch
7
-5,2V
+5V
16
D2
D3
R15
T3
R10
-15V
0
1
+5V
D1
R8
R9
R7
R5
R6
R4
C4
T4
C3
R3
T2
T1
C1
R1
R2
T5
R14
R13
P2
C2
IC1
+15V
R11
P1
R12
+5V
D4
D5
-5,2V
R18
C5
R17
IC2
P5
-15V
+15V
P4
R16
12
R21
P3
R22
-5,2V

FIG 3b